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Study of Adder & Subtractor using OR, EX-OR, AND & NOT Gates Experiment Apparatus

Product Image



Description

Objective : To verify the truth table of Digital Half Adder, Half Subtractor, Full Adder & Full Subtractor using OR, AND, EX-OR & NOT gates.

Features : Instrument comprises of DC Regulated Power Supply 5V/150mA for logic inputs, 4 SPDT switches provided for selecting logic 1 & logic 0 , 2 Red LED output indicators, circuit diagram printed for 1 two input OR gate, 2 two input AND gates, 2 NOT gates & 2 EX-OR gates & their respective ICs placed inside the cabinet & connections brought out at sockets.

Catalog No. Particulars

Disclaimer

The Products details given on this page are indicative in nature and JAPSON reserves the right to change them without prior notice. Buyer is also requested to re-check the specifications and other features of product at the time of order as product development is a continuous process and minor modifications may be made to design based on latest availability, process and design.