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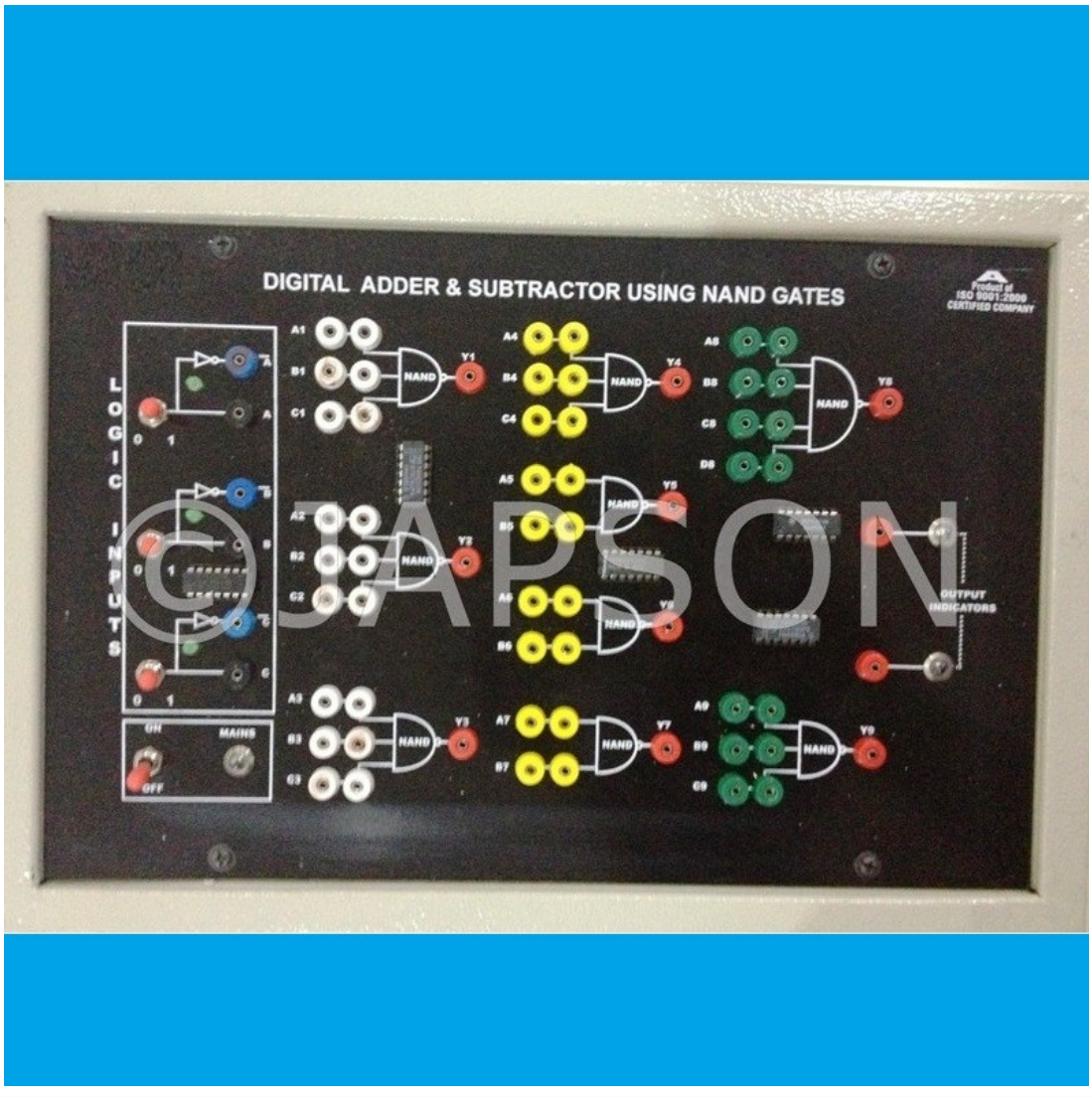
Digital Trainer to Verify Adder & Subtractor using NAND Gate Experiment Apparatus

Product Image



Description

Objective : To verify the truth table of Digital Half Adder, Half Subtractor, Full Adder & Full subtractor using NAND gates.

Features : Instrument comprises of DC Regulated Power Supply 5VDC/150mA for logic inputs, 3 SPDT switches provided for selecting logic 1 & logic 0 , 3 NOT gates for providing compliments of the logic inputs, 2 Red LED output indicator, circuit diagram printed for 5 three input NAND gates, 3 two input NAND gates & 1 four inputs NAND gates & their respective ICs placed inside the cabinet & connections brought out at sockets.

Catalog No.	Particulars
JE21310	Digital Trainer to Verify Adder & Subtractor using NAND Gate Experiment Apparatus

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